In the Claims:

1. (Currently Amended) A memory cell comprising:

a p-well area having at least one NMOS transistor formed therein, the NMOS transistor having an NMOS active area; and

an n-well area having at least one PMOS transistor formed therein; and

wherein the memory cell is a 6T-SRAM memory cell and wherein the memory cell has a long side and a short side, the long side being at least twice as long as the short side, a longitudinal axis of the p-well being parallel to the short side.

2. (Currently Amended) The memory cell of claim 1, wherein the p-well includes at least one pass gate transistor and at least one pull-down transistor sharing a common active area. ~~memory cell is a 6T SRAM cell.~~

3. (Currently Amended) The memory cell of claim [[2,]] 1, wherein maximum resistance between cells p-well to p-well strap contact is less than 4000 ohm.

4. (Currently Amended) The memory cell of claim [[2,]] 1, wherein maximum distance between cells p-well to p-well low resistance strap is less than 3.6 μm.

5. (Currently Amended) The memory cell of claim [[2,]] 1, wherein the p-well area is less than about 65% of the memory cell.

6. (Currently Amended) The memory cell of claim [[2,]] 1, wherein the distance from the n-well area to the NMOS active area is less than about 75 nm.

7. (Currently Amended) The memory cell of claim [[2,]] 1, wherein the NMOS active ~~region~~ area is less than about 25% of the memory cell.

8. (Currently Amended) The memory cell of claim [[2,]] 1, wherein the short side is less than about 0.485 μm.

9. (Currently Amended) ~~The memory cell of claim 1,~~ A memory cell comprising:

a p-well area having at least one NMOS transistor formed therein, the NMOS transistor having an NMOS active area; and

an n-well area having at least two PMOS transistors formed therein; and

wherein the memory cell is an 8T-SRAM [[cell]] cell, wherein the memory cell has a long side and a short side, the long side being at least twice as long as the short side, a longitudinal axis of the p-well being parallel to the short side, wherein a short side of the p-well is shorter than a long side of the p-well, and wherein the PMOS transistors are oriented such that source-to-drain axes of the PMOS transistors are parallel to a longitudinal axis of the n-well, and wherein source/drain regions of the PMOS transistors do not overlap in a direction perpendicular to the longitudinal axis of the n-well.

10. (Original) The memory cell of claim 9, wherein maximum resistance between cells p-well to p-well strap contact is less than 4000 ohm.

11. (Original) The memory cell of claim 9, wherein maximum distance between cells p-well to p-well low resistance strap is less than 3.6 μm.

12. (Original) The memory cell of claim 9, wherein the p-well area is less than about 75% of the memory cell.

13. (Original) The memory cell of claim 9, wherein the distance from the n-well area to the NMOS active area is less than about 100 nm.

14. (Currently Amended) The memory cell of claim 9, wherein the NMOS active area ~~region~~ is less than about 33% of the memory cell.

15. (Original) The memory cell of claim 9, wherein the short side is less than about 0.745 μm.

16. (Original) The memory cell of claim 1, wherein the n-well is a deep n-well.

17. (Original) The memory cell of claim 1, wherein the p-well substantially encircles the n-well.

18. (Original) The memory cell of claim 1, wherein the memory cell includes a plurality of V_{ss} lines, the plurality of V_{ss} lines being located on one or more metal layers.

19. (Original) The memory cell of claim 1, wherein the memory cell has an area of less than about 0.4 μm^2, at least one of the PMOS transistors or the NMOS transistors have a gate thickness less than about 1000 Å.

20. (Original) The memory cell of claim 1, wherein the NMOS transistor has a gate layer and a gate dielectric layer and the gate dielectric layer having one or more layers and at least one

layer comprising SiO_2, nitrided oxide, nitrogen content oxide, SiON, metal oxide, high K dielectric, or a combination thereof.

21. (Original) The memory cell of claim 1, wherein the memory cell includes at least one pull-down transistor having a gate width of less than about 40 nm and a gate dielectric thickness of less than 13 Å.

22. (Original) The memory cell of claim 1, wherein the memory cell has a maximum storage capacitance of less than about 0.5 femto-farad.

23. (Original) The memory cell of claim 1, wherein the memory cell includes at least one bit line, each bit line being parallel to the longitudinal axis of the p-well.

24. (Original) The memory cell of claim 1, wherein the memory cell is formed on a substrate comprising bulk-Si, SiGe, strain-Si, SOI, non-bulk Si, or a combination thereof.

25. (Original) The memory cell of claim 1, wherein the memory cell includes at least one bit line, each bit line having at least one of a V_{cc} line or a V_{ss} line thereof adjacent the bit line.

26. (Original) The memory cell of claim 1, wherein the memory cell includes a plurality of metal layers, and the memory cell includes a bit line and a complementary bit line, the bit line and the complementary bit line being on different metal layers.

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